

ECE3042 Lab Report and Homework Guidelines

Homework

- The first page of the homework is a cover sheet in the specified format.
- Homework is due in lab at the beginning of the period.
- Label all figures/graphs with a descriptive title, i.e. "Gain versus frequency for common emitter amplifier." Don't use the problem number as a title.
- If a graph has multiple traces, each trace must be labeled with a descriptive title, i.e. collector voltage, not V1. You may title and label by hand after printing.
- Make sure that all SPICE plots display the time/date stamp.
- Include the circuit schematic or SPICE deck for each circuit analyzed with SPICE.
- Place your picture on every Multisim, Cadence, and Mathcad assignment.
- Show all calculations and clearly label all numerical results.
- Draw a box around all results.

Lab Report

- Place your picture as the first figure.
- Reports are due at the beginning of the lab period a week after the experiment is performed.
- The lab reports are not formal, but they are organized. They should clearly present your experimental results and any requested calculations.
- The first page of your lab report must be the verification sheet.
- As you complete each procedure in the lab, have your results verified by a lab instructor. You must show the instructor all screen captures and measurements, and you must demonstrate the circuit. You will not receive a check-off with only screen captures.
- To receive full credit on the report, your verification sheet must be signed by your lab instructor, Dr. Brewer, or Dr. Robinson. Instructors for other lab sections or open lab instructors may not sign it. To obtain a signature, you must complete the required number of procedures during your scheduled lab period or work on the experiment for your entire scheduled lab period. It is your responsibility to obtain this signature before leaving the lab.
- An example of the required report format is attached. There are six blocks per page. Each block may contain calculations, plots, or measurements. Each block has a descriptive title. Any calculations associated with a screen capture may be placed in the block with the capture or in an adjacent block. Each screen capture must have a time/date stamp and barcode. Use margins of 0.5" on all sides.

ECE 3042 Check-off Requirements for Experiment 1

Make sure you have made all required measurements before requesting a check-off. For all check-offs, you must demonstrate the circuit or measurement to a lab instructor. All screen captures must have a time/date stamp.

1. Breadboard Preparation

- ✓ Power supply connected to breadboard binding posts.
- ✓ 100 ohm resistors in series with binding posts to positive and negative rails on breadboard.
- ✓ Wire from ground post to ground rail on board.
- ✓ Decoupling capacitors in place and correctly oriented.

4. Bias

- ✓ Collector, base, and emitter voltages and collector current recorded.

5, 6 . Gain and Frequency Response

- ✓ Oscilloscope screen capture showing input and output signals and V_{pp} measurements for each signal.
- ✓ Calculation of the gain.
- ✓ Plot of gain versus frequency made with HPVVEE, LabView, or by hand with -3dB frequencies and midband gain labeled and their values recorded.

7. Clipping

- ✓ Screen capture showing soft clipping on output and measured positive and negative peak amplitudes (can use max and min functions on scope).
- ✓ Screen capture displaying hard clipping on output and measured positive and negative clipping levels (can use max and min functions on scope).
- ✓ Screen capture of XY plot when amplifier is clipped.
- ✓ Calculation of slope of XY plot (use scope cursors).

8. Spectral Analysis

- ✓ Screen capture showing fundamental and distortion components.
- ✓ Screen capture after adjusting pot to maximize amplitude of fundamental but eliminate distortion components.
- ✓ Measured circuit gain after pot adjustment.
- ✓ Measured pot value (disconnect pot from circuit before measuring).

Georgia Institute of Technology

School of Electrical and Computer Engineering

ECE 3042

Microelectronic Circuits Laboratory

Verification Sheet

NAME: _____

SECTION: _____

GT NUMBER: _____

GTID: _____

Experiment 1: Single Stage Amplifier

Procedure	Time Completed	Date Completed	Verification (Must demonstrate circuit)	Points Possible	Points Received
1. Breadboard Prep				20	
4. Bias				20	
5,6. Small Signal Gain and Freq Response				20	
7. Clipping				20	
8. Spectral Analysis				20	

To be permitted to complete the experiment during the open lab hours, you must complete at least **four** procedures during your scheduled lab period or spend your entire scheduled lab session attempting to do so. A signature below by your lab instructor, Dr. Brewer, or Dr. Robinson permits you to attend the open lab hours to complete the experiment and receive full credit on the report. Without this signature, you may use the open lab to perform the experiment at a 50% penalty.

SIGNATURE: _____

DATE: _____

Exp 1. Common Emitter Amplifier

1.6.1. Bias Measurements

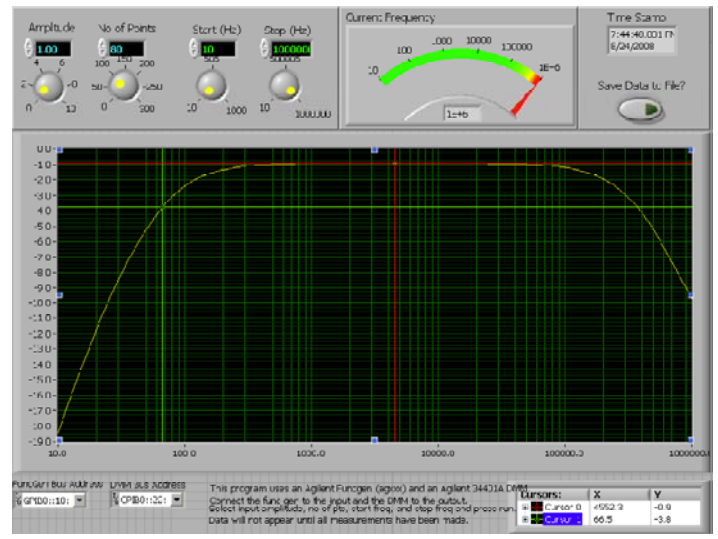
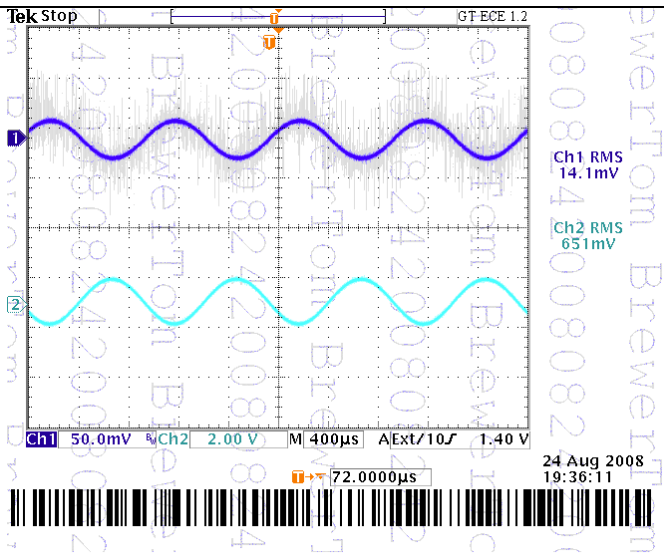


Tom Brewer 1

Collector Voltage = 7.28 V
 Base Voltage = 2.07 V
 Emitter Voltage = 1.42 V
 Collector Current = $(15-7.28)/10k=0.773$ mA

Section 1.6.2. Small Signal Gain Gain=651/14.1=46.2

Section 1.6.3. Frequency Response

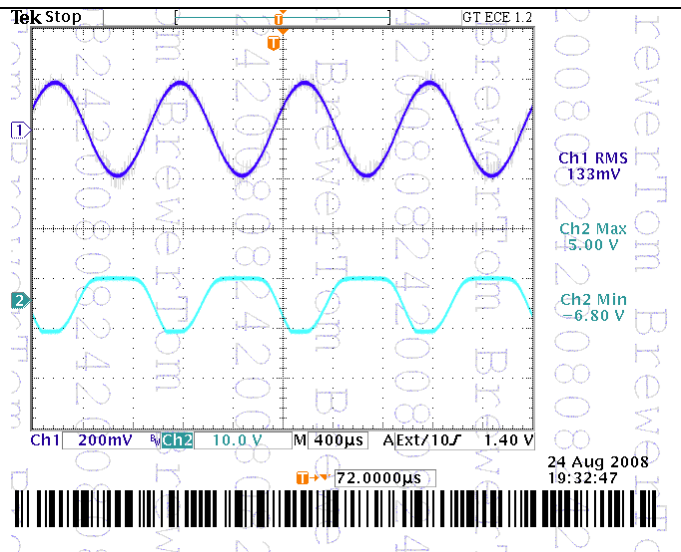


Section 1.6.3. Frequency Response

Section 1.6.4. Large-Signal Clipping Behavior

From Bode Plot:

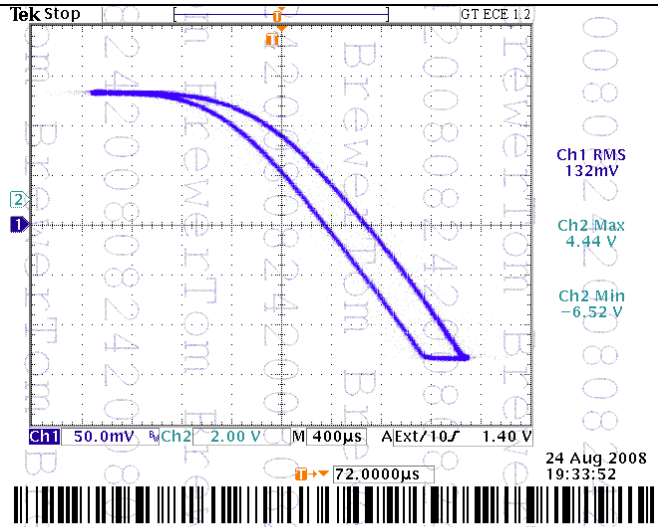
Midband Gain (dB) = $-0.9 + 20\log(1020/20) = 33.25$ Midband Gain (linear) = 46
 Lower 3db = 66Hz
 Upper 3db = 360k



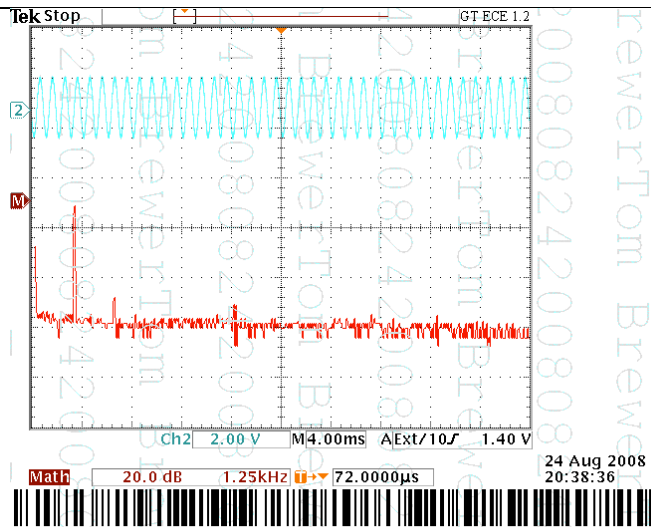
Section 1.6.4. Large-Signal Clipping Behavior

Measured Positive Clipping Level : 5V
 Measured Negative Clipping Level: -6.8V
 Computed Positive Clipping Level: XX
 Computed Negative Clipping Level: XX

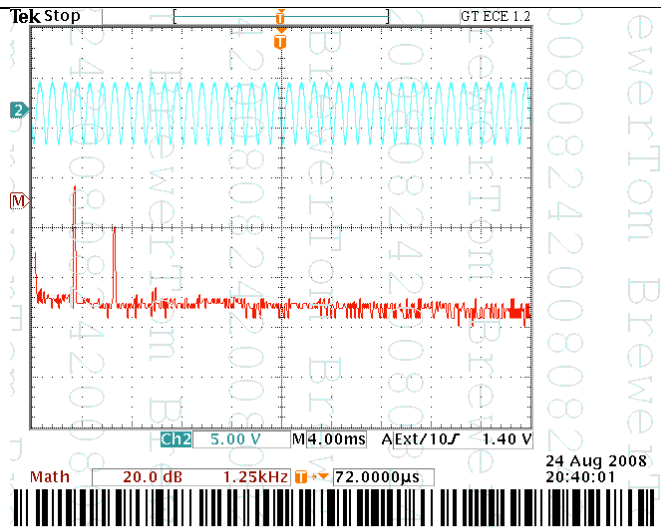
Section 1.6.4. Large-Signal Clipping Behavior Slope = XX



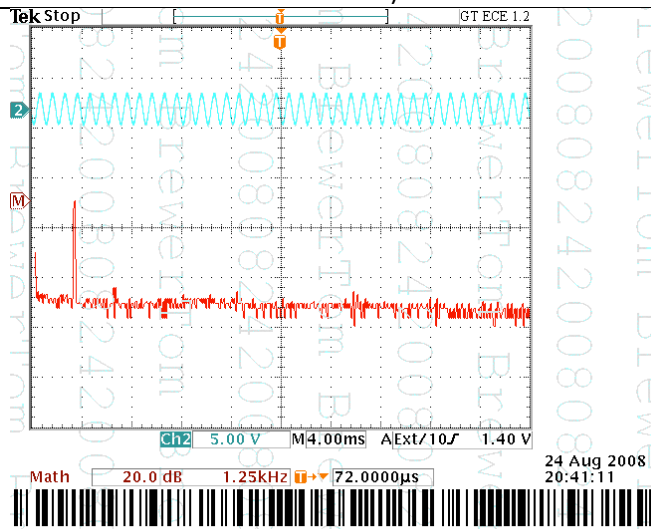
Section 1.6.5. Spectral Analysis (Gain set to 50)



Section 1.6.5. Spectral Analysis (Large second harmonic visible)



Section 1.6.5. Spectral Analysis (Pot set for verge of distortion)



Section 1.6.5. Spectral Analysis (Gain at verge of distortion)
 Av=XX, Rpot = XX

